Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A monolithic semiconductor device comprising:

~~a first encryption engine having an input port;~~

~~a memory location having an output port coupled to the input port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device.~~

a memory location having an output port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device;

an asymmetrical encryption engine having an input port coupled to the output port of the memory location and an output port to provide a symmetrical encryption key based on the data value; and

a symmetrical encryption engine having an input port coupled to an output port of the asymmetrical encryption engine, wherein the symmetrical encryption engine is to perform an encryption function using the symmetrical encryption key.

2. (Currently Amended) The monolithic semiconductor device as in Claim 1, wherein said memory location is observable only to ~~said first~~said asymmetrical encryption engine.

3. (Original) The monolithic semiconductor device as in Claim 1, wherein said memory location is to store an encryption key.

4. (Original) The monolithic semiconductor device as in Claim 1, wherein said memory location includes a register.

5. (Original) The monolithic semiconductor device as in Claim 1, wherein said memory location includes non-volatile memory.

6. (Original) The monolithic semiconductor device as in Claim 5, wherein a value stored in said memory location is defined during a manufacture of the monolithic semiconductor device.

7. (Original) The monolithic semiconductor device as in Claim 6, wherein the value is defined using a lithographic technique.

8. (Original) The monolithic semiconductor device as in Claim 6, wherein the value is defined using a laser etching technique.

9. (Original) The monolithic semiconductor device as in Claim 1, wherein said memory location includes volatile memory.

10. (Canceled)

11. (Currently Amended) The monolithic semiconductor device as in Claim 1, further including:
an external port having an input and an output; and
an isolation portion coupled to the input of said external port and to the output port of said memory location, wherein said isolation portion is to prevent access to said memory location using said external port.

12. (Currently Amended) The monolithic semiconductor device as in Claim 11, wherein said isolation portion includes a fuse coupled between the input of said external port and the output port of said memory location.

13. (Currently Amended) The monolithic semiconductor device as in Claim 1, further including at least one silicon die pad having an input coupled to the output port of said memory location to provide temporary access to said memory location.

14. (Original) The monolithic semiconductor device as in Claim 1, further including a unique ID register coupled to the input of said encryption engine to store a unique ID.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) A monolithic semiconductor device comprising:

an external data port having an input and an output;

a first encryption engine having an input coupled to the input of said external data port and an output;

a second encryption engine having an input coupled to the output of the first encryption engine and an output;

a memory location having an output coupled to the input of said first encryption engine;

an isolation portion coupled to the output of said memory location and to the input of said external data port, wherein said isolation portion is modifiable to permanently prevent access of said memory location by the external data port; and

wherein the first encryption engine is to provide a first encryption key based on a value stored at said memory location to said second encryption engine.

18. (Original) The monolithic semiconductor device as in Claim 17, wherein said memory location includes non-volatile memory.

19. (Currently Amended) The monolithic semiconductor device as in Claim 18, wherein ~~a value~~said value stored in said memory location is defined during a manufacture of the monolithic semiconductor device.

20. (Original) The monolithic semiconductor device as in Claim 19, wherein said value is defined using a lithographic technique.

21. (Original) The monolithic semiconductor device as in Claim 19, wherein said value is defined using a laser etching technique.

22. (Original) The monolithic semiconductor device as in Claim 17, wherein said memory location includes volatile memory.

23. (Canceled)

24. (Original) The monolithic semiconductor device as in Claim 17, wherein said memory location is located in a specific location of the monolithic semiconductor device.

25. (Currently Amended) The monolithic semiconductor device as in Claim 17, wherein said ~~memory location is to store an~~value includes a second encryption key.

26. (Original) The monolithic semiconductor device as in Claim 25, wherein said memory location is to store a plurality of encryption keys.

27. (Currently Amended) The monolithic semiconductor device as in Claim 25, wherein said first encryption engine is to use a portion of ~~the encryption~~the first encryption key to perform an encryption function.

28. (Currently Amended) The monolithic semiconductor device as in Claim 25, ~~further including a second encryption engine having an input coupled to the output port of said first encryption engine, and~~ wherein said first encryption engine is an asymmetrical encryption engine and said second encryption engine is a symmetrical encryption engine.

29. (Currently Amended) The monolithic semiconductor device as in Claim 28, ~~wherein said first encryption engine is to provide a symmetrical encryption key to said second encryption engine~~wherein the first encryption key includes a symmetrical encryption key, and wherein said second encryption engine is to perform an encryption function using the symmetrical encryption key.

30. (Original) The monolithic semiconductor device as in Claim 17, wherein said isolation portion includes a fuse coupled between the input of said external port and the output of said memory location.

31. (Original) The monolithic semiconductor device as in Claim 17, further including at least one silicon die pad coupled to the output of said memory location to provide temporary external access to said memory location.

32. (Original) The monolithic semiconductor device as in Claim 17, further including a unique ID register having an output coupled to the input of said first encryption engine to store a unique ID.

33. (Currently Amended) A method comprising ~~the steps of~~:

accessing, by ~~an encryption engine~~a first encryption engine internal to a monolithic semiconductor device, data from a memory location internal to the monolithic semiconductor device, wherein the memory location is accessible only internal to the monolithic semiconductor device;

generating, at the first encryption engine, a first encryption key based on the data from the memory location;

providing the first encryption key to a second encryption engine internal to the monolithic semiconductor device; and

performing an encryption function ~~using the data~~at the second encryption engine using the first encryption key.

34. (Currently Amended) The method as in Claim 33, wherein the data is accessible only by the first encryption engine.

35. (Currently Amended) The method as in Claim 33, wherein the data represents ~~an encryption~~a second encryption key.

36. (Currently Amended) The method as in Claim 35, further including ~~the steps of~~:

generating the first encryption key; and

providing the first encryption key for storage in the memory location.

37. (Currently Amended) The method as in Claim 33, further including ~~the steps of~~:

accessing externally the data from the memory location; and

isolating the memory location from subsequent external access.

38. (Currently Amended) The method as in Claim 37, wherein ~~the step of~~ accessing externally includes verifying a value of the data.

39. (Currently Amended) The method as in Claim 37, wherein ~~the step of~~ accessing externally includes defining a value of the data.

40. (Currently Amended) The method as in Claim 37, wherein ~~the step of~~ isolating includes blowing a fuse which allows external access to the memory location.

41. (New) A monolithic semiconductor device comprising:

an encryption engine having an input;

a memory location having an output coupled to the input of the first encryption engine, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device;

at least one silicon die pad having an input coupled to the output of said memory location to provide temporary access to said memory location.